THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LANNY E. BOSWELL,
CHRISTOPHER I. MADORE, and MYRON C. BUTLER

Appeal No. 95-4636
Application 08/027,868[1]

ON BRIEF

Before JERRY SMITH, BARRETT and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 6-20. No claim has been allowed.

References relied on by the Examiner

Suzawa	4,487,481	Dec. 11, 1984

[1] Application for patent filed March 8, 1993.

Aoki et al. (Aoki)	4,760,389	July 26, 1988
Butler et al. (Butler)	4,837,811	June 6, 1989
Hilligoss et al. (Hilligoss)	5,025,466	June 18, 1991
Crowdis	5,163,079	Nov. 10, 1992

The Rejections on Appeal

Claims 6 -20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 6, 7, 10 and 14-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Butler and Crowdis.

Claims 8, 9 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Butler and Aoki.

Claims 11-13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Butler and Hilligoss.

Claim 20 stands rejected under 35 U.S.C. § 103 as being unpatentable over Butler and Suzawa.

The Invention

The invention is directed to a data terminal for communications and testing of subscriber equipment in a telephone system of the type having a tip and ring connection. Claim 6 is the only independent claim and reads as follows:

6. A data terminal for communications and testing of subscriber equipment in a telephone system of the type having a tip and ring connection, comprising:

a microprocessor;

an EPROM interconnected with said microprocessor to provide system storage;

dynamic random access memory interactively interconnected with said microprocessor and said EPROM and containing resident MS DOS operating system program;

an address buss interconnected between said microprocessor, said EPROM and said dynamic random access memory;

a data buss interconnected between said microprocessor, said EPROM and said dynamic random access memory;

a field programmable gate array receiving a plurality of control signals, address signals, data signals and sensed signals from around the data terminal, and providing a plurality of gated output signals;

a universal asynchronous receiver-transmitter connected to an 8-bit data buss that interconnects with plural gated output digital data ports from said field programmable gate array and provides output of modem control signals;

telephone line input circuit providing connection to the tip and ring connections of said telephone line and

generating a caller number delivery signal; and

a modem receiving input of said modem control signals and said caller number delivery signal from said telephone line input circuit to provide system subscriber identification.

Opinion

We do not sustain any of the examiner's grounds of rejections of the appellants' claims 6-20 over prior art. We sustain the rejection of claims 6-20 as being indefinite.

The rejection for indefiniteness under 35 U.S.C. § 112, second paragraph

The examiner is correct that the term "said telephone line" in claim 6 is without antecedent basis. Although the problem is easily correctable, it does render the claimed subject matter vague and indefinite because that which is referred to does not exist. The appellants indicate that they intend to amend the language to refer instead to "said telephone system" if the claim is otherwise allowable. In our view, if so amended, the problem would be corrected. However, before us is the claim in its present form. Accordingly, we sustain the rejection of claim 6 as being indefinite under 35 U.S.C. § 112, second paragraph.

The examiner regards claim 7 as indefinite because it does not recite any means for selecting a communication channel and because it is not clear between what entities does the communication channel exist. Claim 7 depends from claim 6 and reads as follows:

7. A data terminal as set forth in claim 6 which further includes:

> a digital to analog converter connected to said 8-bit
> data buss and producing an analog control signal indicative of a selected communication channel.

In our view, the examiner's positions are without merit. The appellants need not recite in the claims every functional part of an operational device. All that is required by claim 7's language at issue is an analog control signal which is "indicative of a selected communication channel." Not specifying precisely what it is that does the selection merely makes the claim broad, not indefinite, and the same is true as to not knowing between which entities is the communication channel selected. Breadth does not equate to indefiniteness. In re Miller, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971); In re Gardner, 427 F.2d 786, 166 USPQ 138 (CCPA 1970).

However, because all the claims depend from claim 6 and thus include all the limitations of claim 6, the indefiniteness of claim 6 renders all the claims indefinite. Accordingly, we sustain the rejection of claims 7-20 as being indefinite under 35 U.S.C. § 112, second paragraph.

If claim 6 is amended to overcome its lack of antecedent basis problem, claims 7-20 would no longer be indefinite.

The obviousness rejections of
claims 6-20 under 35 U.S.C. § 103

We do not sustain the rejection of claims 6, 7, 10 and 14-18 over Butler and Crowdis. We do not sustain the rejection of claims 8, 9 and 19 over Butler and Aoki. We do not sustain the rejection of claims 11-13 over Butler and Hilligoss. We do not sustain the rejection of claim 20 over Butler and Suzawa.

Butler is the base or primary reference for all of the prior art type grounds of rejections. As will be discussed below, the manner in which the examiner has applied the teachings of Butler to the claimed invention entailed several deficiencies.

The examiner correctly found that Butler discloses a microprocessor, an EPROM, a RAM, an address bus, a data bus, a UART and a modem. See Butler's Figure 1, components 10, 26 and 28. Butler does not disclose a circuit generating a caller number delivery signal which is received by the modem. However, Crowdis does, and the examiner is correct in concluding that it would have been obvious to one with ordinary skill in the art, in light of Crowdis, to have such a caller number delivery circuit in the system of Butler. In

that regard, we reject the appellants' argument: "While it is true that the Crowdis patent also teaches the similar function, the caller ID number is retrieved through the FPGA circuitry in Applicants' data terminal." The appellants have not shown where in any rejected claim is the requirement that the caller ID number is retrieved through the FPGA circuitry.

What Butler clearly does not disclose is the claimed field programmable gate array (FPGA) which receives a plurality of control signals, address signals, data signals, and sensed signals from around the data terminal, and provides a plurality of gated outputs. Moreover, according to claim 6, the UART must be connected to an 8-bit data bus which connects to the plural gated output digital ports from the field programmable gate array.

With regard to the "FPGA" feature of the invention, the examiner states (answer at 5):

> FPGAs are again well known in the art for allowing the user to program an integrated circuit to a specific need such as generation of complex logic functions as an alternative to more expensive applications specific integrated circuits. The number and order of FPGAs, and the number of resident logic gates is apparently an obvious matter [of] design that will depend on the [a] system requirement. Thus, it would have been obvious to one of ordinary skill in the art at the time the

> invention was made to use an FPGA in place of a cascade of separate logic gates for connecting the CPU and memories used by Butler et al. as shown in Figs. 4 and 5 for the purpose of using a standard, off-the-shelf circuits for programming special functions as desirable.

Figure 5 of Butler does show several logic circuits, i.e., decoders 150 and 156 and data selector 138, each of which indeed can be implemented by an FPGA circuit. However, the examiner evidently has overlooked a difference between the appellants' claimed invention and Butler.

In Butler, the overall system architecture is particularly illustrated in its Figure 1. As shown, there is no system component positioned between the computer 10 (CPU, RAM and EPROM) and the UART 26. Thus, whatever circuitry the examiner proposes to implement by FPGA instead of the disclosed implementation in Butler is not disposed between the computer 10 and the UART 26 as is required by the appellants' claim 6. Butler's Figures 4 and 5 evidently do not show the UART or how it is connected to the various circuit which are shown. The examiner has articulated no reasonable motivation for one with ordinary skill in the art to add another layer of

circuitry between the computer 10 and the UART 26 in Butler, much less such a layer comprising an FPGA.

The examiner has resorted to speculation to account for the necessary connection between the FPGA and the UART. The examiner first proposes to change certain unspecified logic gates of Butler to an FPGA, and then concludes that the connection of the UART to the FPGA would follow (answer at 11). According to the examiner, an FPGA implementation of Butler's data terminal would inevitably result in the appellants' claimed invention, and the data bus of the UART "must be" connected to the data ports of the FPGA (answer at 12). The conclusion is not supported by the evidence of record and amounts to speculation. Again, it is noted that Figures 4 and 5 of Butler do not illustrate how the various detailed circuitry is connected to the UART identified in Figure 1. The examiner may not, because he or she may doubt the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis supporting the rejection. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). The filling in of the

gaps in the reference, in this case, also cannot be justified on the basis of official notice. As is stated in In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970):

> Assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellants given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference. (Citations omitted.)

Additionally, note that the examiner has not even identified what exactly is an "FPGA" implementation of Butler's data terminal; it is uncertain what the examiner has proposed to substitute with a FPGA. The FPGA according to the claimed invention must receive a plurality of the following signals from around the data terminal: control signals, address signals, data signals, and sensed signals. In our view, the examiner appears to have speculated with respect to this feature as well.

We reject the appellants' argument that it would not have been obvious to one with ordinary skill in the art to use MS DOS as the operating system for the claimed data terminal. The examiner is correct that a well known operating system such as MS DOS would have been recognized by one with ordinary

skill in the art as being usable for the data terminal. Nonetheless, the rejection of the claims is without merit because of the deficiencies relating to the FPGA aspect of the invention.

In light of the foregoing deficiencies, it cannot be said that the examiner has presented a prima facie case of obviousness. Claim 6 is the only independent claim. All of the other claims depend, either directly or indirectly from claim 6. The references Aoki, Hilligoss, and Suzawa all have been relied upon by the examiner only for meeting the additional features recited in the respective dependent claims and not for meeting the FPGA feature recited in independent claim 6. Therefore, the other references do not make up for the deficiencies of Butler.

For the foregoing reasons, the rejection of claims 6-20 under 35 U.S.C. § 103 as being unpatentable over Butler in various combinations with Crowdis, Aoki, Holligoss, and Suzawa cannot be sustained.

Conclusion

The rejection of claims 6-20 under 35 U.S.C. § 112, second paragraph, as being indefinite is affirmed.

The rejection of claims 6, 7, 10 and 14-18 under 35 U.S.C. § 103 as being unpatentable over Butler and Crowdis is reversed.

The rejection of claims 8, 9 and 19 under 35 U.S.C. § 103 as being unpatentable over Butler and Aoki is reversed.

The rejection of claims 11-13 under 35 U.S.C. § 103 as being unpatentable over Butler and Hilligoss is reversed.

The rejection of claim 20 under 35 U.S.C. § 103 as being unpatentable over Butler and Suzawa is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JERRY SMITH Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JAMESON LEE Administrative Patent Judge	)	

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